SISC 2024

55th IEEE
Semiconductor Interface
Specialists Conference

December 11–14, 2024
Catamaran Resort Hotel and Spa, San Diego, CA
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# IEEE SISC 2024

# CONFERENCE PROGRAM

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# SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, "MOS Physics and Technology," published by Wiley Interscience.

The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author for either an oral or a poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

## 2023 SISC Ed Nicollian Award for Best Student Paper

**Rehan Younas**

*University of Notre Dame*

"Ferromagnetism in Tungsten Diselenide and the Role of Selenium Vacancies"
with G. Zhou, X. Liu, S. Tiwari (UT Dallas), W. G. Vandenberghe (UT Dallas),
B. Assaf, and C. L. Hinkle

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# SISC T. P. Ma Award for Best Student Poster

In 2021, the SISC added an award for the best student poster in honor of Professor T. P. Ma, Yale University. Professor Ma was an internationally recognized pioneer for his contributions to semiconductor science and technology — in particular, breakthroughs in advanced gate dielectrics, which paved the path for high-$\kappa$ dielectrics and extended the scaling of CMOS technology. His research also generated fundamental and lasting impacts on many other applied physics fields, notably ferroelectrics and ionizing radiation sciences.

The *SISC T. P. Ma Award* will be presented to the lead student author for a poster presentation. The winner will be chosen by members of the technical program committee at the end of the SISC. The award will consist of a plaque, an honorarium, and a permanent mention on the conference web site.

## 2023 SISC T. P. Ma Award for Best Student Poster

**Shreyam Natani**

*University of California, San Diego*

"Conformal, ultrathin top gate oxide for monolayer $MoS_2$"
with M. Passlack (TSMC), I. Radu (TSMC), A. C. Kummel, and P. Bandaru

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# Wednesday Evening Tutorial

## Wednesday, December 11, 2024, 8:00 PM

First introduced at SISC 2008, the Wednesday Evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

# Hafnia-Based Ferroelectric FETs and Capacitors for Low-Power Memory and AI Applications: Physical Understanding of Device Operation and Reliability

**Prof. Shinichi Takagi,** *U. Tokyo, Japan*

Since the discovery of ferroelectricity in $HfO_2$-based dielectric films in 2011, ferroelectric devices using $HfO_2$-based thin films as dielectrics have attracted strong interest. Thus, active research and developments on Si-friendly $HfO_2$-based ferroelectric FeRAMs and FeFETs have been conducted for memory and logic applications with extremely low power consumption. Furthermore, these $HfO_2$-based ferroelectric devices are also promising as hardware for realizing AI applications with high energy efficiency, because of the versatile properties such as analog memory characteristics and coexistence of memory and logic functions.

This tutorial will introduce the recent development of FeRAMs and FeFETs for memory and AI applications with an emphasis on the physical understanding of electric characteristics and reliability. For metal/ferroelectric/metal (MFM) capacitors, I will provide the critical issues for FeRAM applications, such as ferroelectric film thickness scaling, operation voltage and reliability including oxide breakdown, wakeup and fatigue. Also, for metal/ferroelectric/semiconductor (MFIS) gate stacks, I will discuss the complicated interaction and coupling between polarization charges, trapped charges and inversion-layer charges, which are of the paramount importance in quantitative understanding of the FeFET operation and the reliability. Based on this knowledge, the memory characteristics and the reliability of FeFETs will be examined from the viewpoint of the ferroelectric film thickness scaling.

The tutorial will also explore the AI applications using the $HfO_2$-based ferroelectric devices. Various examples of the ferroelectric devices for application to AI computation systems will be introduced. Among them, this presentation will shed light more on physical reservoir computing using FeFETs, which is one of the unique AI computation

applications that take advantage of the ferroelectric device properties. Physical reservoir computing, represented by hardware with input-history-dependent and nonlinear dynamics, has recently attracted significant attention as a method to realize real-time AI processing with high energy efficiency at the edge. The principle, the basic AI characteristics and applications to speech recognition of FeFET reservoir computing will be explained.

## Biography

*Shinichi Takagi received B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1982, 1984, and 1987, respectively. He joined the Toshiba Research and Development Center, Japan, in 1987, where he was engaged in research on the device physics of Si MOSFETs. From 1993 to 1995, he was a Visiting Scholar at Stanford University, where he studied Si/SiGe hetero-structure devices. In October 2003, he moved to the University of Tokyo, where he is currently working as a professor in the Department of Electrical Engineering and Information Systems. He has authored and co-authored more than 420 papers in technical journals and more than 780 papers in international conferences. Also, he has received 18 awards including the IEEE Paul Rappaport Award (2014), IEEE Andrew S. Grove Award (2013), IEEE George E. Smith Award (2003), and the Purple Ribbon Medal from the Japanese government (2017). His recent interests include the science and technologies of advanced CMOS devices using Ge and III-Vs, ferroelectric devices, and cryo-CMOS.*

*Prof. Takagi has served on the technical program committee of several international conferences including IEDM, Symposium on VLSI Technology, IRPS, SSDM, and ISSCC. He is a member of the IEEE Electron Device Society, the Institute of Electronics, Information, and Communication Engineers (IEICE), and the Japan Society of Applied Physics (JSAP).*

# Invited Honorary Lecture

## Friday, December 13, 2024, 3:50 PM

Prof. Stesmans has been attending SISC unwaveringly from 1988 until and even past his retirement. He is currently the longest attending SISC participant. His fundamental work on the identification of point defects at the $Si/SiO_2$ interface through electron spin resonance (ESR), and on the accurate description of their complex passivation kinetics in hydrogen ambient has been instrumental for the semiconductor industry, and it still proves immensely valuable for the current advanced logic integration endeavors. We are delighted to host Prof. Stesmans at SISC 2024, delivering an honorary lecture about his seminal research.

# Electron spin resonance as powerful spectroscopy for assessment of point defects in semiconductor/insulator structures: some historical reflections on interfaces

**Prof. Andre Stesmans,** *U. Leuven, Belgium*

## Biography

*Andre Stesmans obtained his PhD in Physics at KU Leuven in 1977. In 1979 he started a permanent position as researcher with the FWO Belgium, and the same year he took up a faculty position as associate professor in the Physics Department at KU Leuven, where he serves as full professor in physics since 1991. His past research interests have included the size effect on electronic transport in metals at cryogenic temperatures and the application of magnetic resonance to the study of conduction electrons, during which research activity he has stayed at the Universities of Exeter (UK), Detroit (USA), and Lanzhou (China). His current main research interest is situated in semiconductor physics, in particular fundamental characterization of interfaces and surfaces of low dimensional semiconductor/insulator heterostructures by the electron spin resonance technique in conjunction with electrical characterization.*

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IEEE ELECTRON DEVICES SOCIETY

# Conference Agenda Overview

## Wednesday, December 11, 2024

| | |
|---|---|
| **Registration** | 7:00 PM – 8:00 PM |
| **Evening Tutorial** | 8:00 PM – 9:30 PM |

## Thursday, December 12, 2024

| | |
|---|---|
| **Registration** | 8:00 AM – 5:00 PM |
| **Session 1: Amorphous Oxide Semiconductors: IGZO** | 8:25 AM – 10:20 AM |
| **Session 2: Amorphous Oxide Semiconductors: other channels** | 10:35 AM – 12:15 PM |
| **Session 3: 2D channels** | 1:30 PM – 3:20 PM |
| **Session 4: Poster Preview Session II: Advanced Logic, 2D, Ferroelectrics, Emerging Memory** | 3:20 PM – 3:45 PM |
| **Session 5: Ferroelectrics I** | 4:00 PM – 5:35 PM |
| **Session 6: Poster Preview Session II: Amorphous Oxide Semiconductors, Wide Bandgap, Thin Films, Interconnects** | 5:35 PM – 6:00 PM |
| **Reception & Poster Session** | 7:00 PM – 10:00 PM |

## Friday, December 13, 2024

| | |
|---|---|
| **Registration** | 8:00 AM – 12:00 PM |
| **Session 7: Ferroelectrics II** | 8:30 AM – 10:40 AM |
| **Session 8: Advanced Logic I** | 10:55 AM – 12:05 PM |
| **Committee / Invited Speaker Luncheon (by invitation only)** | 12:10 PM – 1:55 PM |
| **Session 9: Advanced Logic II** | 2:00 PM – 3:30 PM |
| **Session 10: Defects** | 3:45 PM – 5:45 PM |
| **Conference Banquet & Limerick Contest** | 7:00 PM – 10:00 PM |

## Saturday, December 14, 2024

| | |
|---|---|
| **Session 11: Emerging Memory** | 8:30 AM – 10:00 AM |
| **Session 12: Wide Bandgap Semiconductors** | 10:15 AM – 12:15 PM |

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## Wednesday, December 11, 2024

### Tutorial

Session Chair: J. Franco

8:00 PM – 9:30 PM *Tutorial* – **Hafnia-Based Ferroelectric FETs and Capacitors for Low-Power Memory and AI Applications: Physical Understanding of Device Operation and Reliability,** Shinichi Takagi, *U. Tokyo, Japan*

## Thursday, December 12, 2024

### Session 1: Amorphous Oxide Semiconductors: IGZO

Session Chair: TBD

8:25 AM **Opening Remarks,** J. Rozen, *IBM*

8:30 AM 1.1 *Invited* – **IGZO thin-film transistor reliability: the last standing roadblock for memory applications,** A. Chasin, *imec, Belgium*

9:00 AM 1.2 – **In-situ Fluorine Doped IGZO FETs with Enhanced Hydrogen Immunity,** Q. Kong, C. Sun, G. Liu, Y. Chen, W. Shi, Z. Zheng, L. Jiao, Z. Zhou, and X. Gong, *National U. of Singapore, Singapore*

9:20 AM 1.3 – **IGZO Transistors with Hydrogen Reservoir Pd Source/Drain,** Z. Lin, Y. Zhang, D. Chen, X. Li, X. Zhao, and M. Si, *Shanghai Jiao Tong U., China*

9:40 AM 1.4 – **Selective Defect Annihilation for Nanoscale Self-Aligned Source/Drain of InGaZnO Thin-Film Transistors,** Jiye Li, T. Huang, Y. Zhang, Jinxiong Li, X. Wang, Z. Wang, Y. Cai, L. Lu, and S. Zhang, *Peking U., China*

10:00 AM 1.5 – **Electron trap density extraction in scaled IGZO TFTs from frequency-dependent admittance measurements,** H. Tang[1,2], A. Belmonte[1], D. Lin[1], A. Chasin[1], S. Subhechha[1], Y. Wan[1], H. Dekkers[1], J. Li[1], Z. Chen[1,2], G. S. Kar[1], J. Van Houdt[1,2], and V. V. Afanas'ev[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

10:20 AM Coffee break

## Session 2: Amorphous Oxide Semiconductors: other channels

Session Chair: TBD

10:35 AM — 2.1 – **Performance Enhancement of PEALD-$In_2O_3$ BCE TFTs and GAA Nanosheet FETs by Oxygen Supercritical Fluid Passivation,** Y.-S. Wu[1], C.-W. Kuo[2], Y.-M. Liu[1], J.-C. Chiu[1], J. Gracia[1], R.-W. Ma[1], H. Fujiwara[1], Y.-C. Fan[1], H.-M. Sung[1], T.-C. Chang[2], and C. W. Liu[1], [1]*National Taiwan U., Taiwan,* [2]*National Sun Yat-Sen U., Taiwan.*

10:55 AM — 2.2 – **The Critical Role of Degenerate Semiconductor in Temperature-Insensitive Device Performance: Ultrathin $In_2O_3$ Transistors,** J. -Y. Lin[1], C. Niu[1], T. Kim[2], B. Park[2], H. Jang[2], C. Jeong[2], and P. D. Ye[1], [1]*Purdue U.,* [2]*Ulsan National Institute of Science and Technology, Korea*

11:15 AM — 2.3 – **Enhancement of $In_2O_3$ Field-Effect Mobility Using Scaled $Hf_xZr_{1-x}O_2$-Based Higher-κ Linear Dielectric by Strain Engineering,** Z. Lin and P. D. Ye, *Purdue U.*

11:35 AM — 2.4 – **Ultra-low $I_{off}$ of $In_2O_3$:W (IWO) FET and High Field-Effective Mobility of $In_2O_3$ FET for 2T0C eDRAM with 2-bit Endurance >$10^{10}$ cycles and Retention >10 s Toward M3D/BOEL-Compatible Technology,** Z.-F. Lou[1], K.-C. Buu[1], C.-C. Cheng[1], H. Liu[1], Y.-T. Chang[1], K.-Y. Hsiang[2], C.-H. Liu[1], P.-Y. Li[1], S. Maikap[3], Y.-L. Yeh[4], M.-H. Liao[1], I.-C. Cheng[1], and M.-H. Lee[1]., [1]*National Taiwan U., Taiwan,* [2]*National Yang Ming Chiao Tung U., Taiwan,* [3]*Chang Gung U., Taiwan,* [4]*Powerchip Semiconductor Manufacturing Corporation, Taiwan*

11:55 AM — 2.5 – **Amorphous $TeO_2$ as P-type Oxide Semiconductor for BEOL Devices,** J. Robertson[1], X. Zhang[1], Q. Gui[2], and Y. Guo[2], [1]*Cambridge U., UK,* [2]*Wuhan U., China*

12:15 AM — Adjourn for lunch

## Session 3: 2D channels

Session Chair: TBD

1:30 PM — 3.1 *Invited* – **Monolithic 3D Integration of Functionally Diverse 2D Devices,** S. Das, *Pennsylvania State U.*

2:00 PM — 3.2 – **Impact of gate stack scaling and optimization on carrier transport in monolayer $MoS_2$ MOSFETs,** M. Introna[1,2], X. Wu[1], D. Cott[1], Z. Lin[1,2], P. Morin[1], P. Kumar[1], H. M. Silva[1], C. J. Dorow[3], A. Kitamura[3], K. P. O'Brien[3], S. B. Clendenning[3], U. Avci[3], L. Goux[1], C. J. L. de la Rosa[1], G. S. Kar[1], K. Banerjee[1], V. V. Afanas'ev[1,2], and D. Lin[1], [1]*imec, Belgium,* [2]*U. Leuven, Belgium,* [3]*Intel*

2:20 PM — 3.3 – **Observation of Fully Recoverable Breakdown-like Leakage in $HfO_2$ Gate Oxide of $WS_2$ 2D FETs Induced by Local Mechanical Stress,** K. Vishwakarma[1,2], B. Kaczer[1], Q. Smets[1], L. Panarella[1,2], A. Kruv[1], M. Gonzalez[1], O. O. Okudur[1], Y. Yao[1], and I. De Wolf[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

2:40 PM — 3.4 – **$MoTe_2/SiO_2$ Interface Electron Band Alignment: Impact of 2H to 1T′ Polytype Transition,** P. P. Tummala[1,2,3], V. V. Afanas'ev[2,4], G. Ferrini[3], C. Martella[1], A. Molle[1], and A. Lamperti[1], [1]*CNR Institute for Microelectronics and Microsystems, Italy,* [2]*U. Leuven, Belgium,* [3]*UC Sacro Cuore, Italy,* [4]*imec, Belgium*

3:00 PM 3.5 – **Identification of defects on monolayer $MoS_2$ through infrared photo-induced force microscopy,** S. Natani[1], S. Park[2], A. C. Kummel[1], and P. Bandaru[1], [1]*UCSD,* [2]*Molecular Vista, Inc.*

## Session 4: Poster Preview Session I: Advanced Logic, 2D, Ferroelectrics, Emerging Memory

Session Chair: TBD

3:20 PM 4.1 – **High Performance Ge FinFET CMOS Devices with Post Plasma Oxidation and Nitridation Treatments Before Supercritical Fluid Process,** Y.-C. Huang[1], D.-B. Ruan[2], K.-S. Chang-Liao[1], and K.-C. Yang[1], [1]*National Tsing Hua U., Taiwan,* [2]*Fuzhou U., China*

3:21 PM 4.2 – **Understanding of Channel Profile Impact of Fin-based Flip-FET,** J. Sun, H. Lu, W. Peng, and H. Wu, *Peking U., China*

3:22 PM 4.3 – **Advanced TCAD modeling to predict scaling limitations of $MoS_2$ FETs with thin gate insulators,** Y. Z. Lv, Y. J. Chai, and Y. Y. Illarionov, *Southern U. of Science and Technology, China*

3:23 PM 4.4 – **The First Direct Evidence of Interfacial Structure of FeFET With TiN/$Hf_{0.5}Zr_{0.5}O_2$/$SiO_x$/Si Gate Stacks by Atomic-scale Physical Characterization,** X. Z. Shao[1,2], H. Xu[1], S. F. Dai[1,2], X. Y. Ke[1], F. B. Tian[1,2], M. Liao[1,2], H. Y. Fan[1,2], X. Q. Sun[1], J. S. Chai[1], X. Wang[1], and W. W. Wang[1], [1]*Chinese Academy of Sciences, China,* [2]*U. of Chinese Academy of Sciences, China*

3:24 PM 4.5 – **Impact of Top $SiO_2$ Interlayer Thickness on Memory Window of Si Channel Ferroelectric Field-Effect Transistors with MIFIS Gate Structure,** T. Hu, X. Z. Shao, X. P. Jia, M. K. Bai, J. S. Chai, H. Xu, and X. Wang, *Chinese Academy of Sciences, China*

3:25 PM 4.6 – **Low Frequency Noise Measurements on a III-V Gate-All-Around Nanowire Ferroelectric Transistor,** Z. Zhu, M. K. Ram, A. E. O. Persson, and L.-E. Wenersson, *Lund U., Sweden*

3:26 PM 4.7 – **Seed-Induced Lateral Crystallization of Sub-5 nm $Hf_{0.5}Zr_{0.5}O_2$ via Low Thermal Budget for Next-Generation 3D Architectures,** S. Kim[1], T. H. Moon[2], and W. J. Jeon[1], [1]*Kyung Hee U., Korea,* [2]*Ajou U., Korea*

3:27 PM 4.8 – **Enhanced Thermal Stability in Asymmetric $HfO_2$-$ZrO_2$-$HfO_2$ Superlattice Gate Stacks,** H. Lyu[1,2], K. Zhong[1,2], Z. Zhang[1,2], and H. Yin[1,2], [1]*Chinese Academy of Sciences, China,* [2]*U. of Chinese Academy of Sciences, China*

3:28 PM 4.9 – **Modeling Single-Event-Effects in Silicon Bulk FeFET,** S. E. Wodzro, O. Phadke, S. Datta, and S. Yu, *Georgia Tech*

3:29 PM 4.10 – **Interface reactions in ferroelectric $RuO_2$/HZO devices: $RuO_2$ reduction upon annealing,** N. Patel, A. Irish, R. Jones, R. Athle, M. Borg, and R. Timm, *Lund U., Sweden*

3:30 PM 4.11 – **Thickness Scaling Effects on Device Performance and Structural Transformations in Flash Annealed HZO-based Capacitors via Time-resolved Synchrotron X-ray Diffraction,** C. E. Ruano Arens[1], B. Saini[1], V. Thampy[2], D. Van Campen[2], P. C. McIntyre[1,2], and J. D. Baniecki[2], [1]*Stanford U.,* [2]*SLAC National Accelerator Laboratory*

3:31 PM 4.12 – **$O_2/N_2$ Plasma Treatment on the Interfacial Layer of Ferroelectric FETs Gate Stack,** S. Yang[1,2], Y. Raffel[1], D. Lehninger[1], F. Schöne[1], K. Seidel[1], M. Lederer[1], and G. Gerlach[2], [1]*Fraunhofer IPMS-CNT, Germany,* [2]*TU Dresden, Germany*

3:32 PM 4.13 – **Improved Ferroelectric Tunnel Junction Memory Characteristics Using Thin $TiN_x$ Interfacial Capping Layer on $Hf_{0.1}Zr_{0.9}O_2/Al_2O_3$ Tunneling Oxide,** S. Maikap[1,2], A. Senapati[1], Z.-F. Lou[3], Y.-P. Chen[1,2], S.-Y. Huang[1,2], C. W. Liu[3], and M.-H. Lee[3], [1]*Chang Gung U., Taiwan,* [2]*Chang Gung Memorial Hospital, Taiwan,* [3]*National Taiwan U., Taiwan*

3:33 PM 4.14 – **Non-Volatile Charge-Trap Memory Characteristics with Low-Temperature Atomic Layer Deposited $HfO_{2-x}$ Charge-Trap Layer and Enhanced Hole Trapping by Rapid Thermal Annealing,** T. Noh, J. Han, J. Ryu, J.-G. Park, and T.-S. Yoon, *Ulsan National Institute of Science and Technology, Korea*

3:34 PM 4.15 – **A mempolar transistor made from tellurium,** Y. Yang[1], L. Xu[2], M. Xu[3], H. Liu[1], D. Liu[1], W. Duan[4], J. Pei[1], and H. Li[1], [1]*Tsinghua U., China,* [2]*Dongfang Jingyuan Electron Ltd., China,* [3]*Guangdong Institute of Intelligence Science and Technology, China,* [4]*Beijing Information Science and Technology U., China*

3:35 PM 4.16 – **SU-8 Passivated IGZO-Based RRAM on Foldable PET Substrate Stabilizing Endurance and Retention Characteristics Against Bending Stress,** S. Gora, M. Jangra, J. Singh, H. Vaibhav, and A. Datta, *IIT Roorkee, India*

3:36 PM 4.17 – **Band Energies in $ZrO_2$/a-$Al_2O_3$/$ZrO_2$ DRAM Capacitors: a Quantum Confinement Effect,** R. Cao and J. Robertson, *Cambridge U., UK*

3:37 PM 4.18 – **Forming-Free, Low-Voltage, and Two-Step Resistance Change in Ag/$VO_x$/Pt RRAM by Ag Filament Formation for Unconventional Computing Systems,** J. Ryu, J. Han, J.-G. Park, and T.-S. Yoon, *Ulsan National Institute of Science and Technology, Korea*

3:38 PM 4.19 – **Stress Electrical Forming Operation Scheme on ZnO-based RRAM for Emerging Memory Applications,** Y. Huang[1], L. Jiang[2], M. Marander[3], S. Jiang[3], H. Qin[2], J. M. Jones[4], C. Hills[4], and Y. Chen[1], [1]*Arizona State U.,* [2]*U. of Wisconsin,* [3]*Iowa State U.,* [4]*NASA Marshall Space Flight Center*

3:39 PM 4.20 – **Charge-Trap Memory Characteristics in MOS Capacitors with Oxygen-Deficient and Nitrogen-Doped Tantalum Oxide as a Charge-Trap Layer,** J.-G. Park, J. Han, J. Ryu, and T.-S. Yoon, *Ulsan National Institute of Science and Technology, Korea*

3:40 PM 4.21 – **Weight-Update Characteristics Dependent on a Load Resistance of Sub-Threshold Synaptic Pass-Transistors with a Hf-doped ZnO Channel Layer,** D. Cha, J. Pi, S. Byun, G. Do, N. Lee, K. Tae, H. Kim, and S. Lee, *Pusan National U., Korea*

3:41 PM 4.22 – **Tunnel barrier Isolated Stacked cladded Quantum Dots for Multi-state Logic at sub-milliKelvin and Compute-In Memory Applications,** A. F. Jain[1], B. R. H. Gudlavalleti[2], C. J. Chandy[3], and D. E. Heller[4], [1]*U. of Connecticut,* [2]*Synopsys Inc.,*

3:45 PM Coffee break

## Session 5: Ferroelectrics I

Session Chair: TBD

4:00 PM — Limerick contest introduction

4:05 PM — 5.1 *Invited* – **Variability in Hafnia-based Ferroelectrics: A Phase-Field Simulation based Perspective,** S. Gupta, *Purdue U.*

4:35 PM — 5.2 – **C-axis Oriented $Hf_{0.5}Zr_{0.5}O_2$ on Flat TiN Achieving High Remanent Polarization, High Breakdown Field, and Endurance >4E12,** Y.-T. Liao, Z. Zhao, Y.-R. Chen, Y.-W. Chen, W.-H. Hsieh, J.-F. Wang, Y.-A. Chen, H.-Y. Lu, W.-T. Hsu, and C. W. Liu, *National Taiwan U., Taiwan*

4:55 PM — 5.3 – **Fundamental Insight into Non-linear Dielectric Response in Ferroelectric Capacitors to Understand and Improve the Capacitive Memory Window for Non-destructive Read,** S. Mukherjee[1,2], P. Roussel[1], J. Bizindavyi[1], S. Clima[1], M. I. Popovici[1], Y. Xiang[1], A. Belmonte[1], G. S. Kar[1], V. V. Afanas'ev[1,2], and J. Van Houdt[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

5:15 PM — 5.4 – **Temperature-Dependent Switching and Structural Changes in Ultra-Thin Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Capacitors,** B. Saini[1], C. R. Arens[1], V. Thampy[2], J. D. Baniecki[2], W. Tsai[1], and P. C. McIntyre[1,2], [1]*Stanford U.,* [2]*SLAC National Accelerator Laboratory*

## Session 6: Poster Preview Session II: Amorphous Oxide Semiconductors, Wide Bandgap, Thin Films, Interconnects

Session Chair: TBD

5:35PM — 6.1 – **Enhancing Electrical Properties of $ZrO_2$-Based DRAM MIM Capacitors through $In_2O_3$ Doping,** J. H. Jeong[1], S. Lee[1], Y. A. Choi[1], D. H. Kim[2], H. S. Oh[2], Y. J. Park[2], and W. J. Jeon[1], [1]*Kyung Hee U., Korea,* [2]*SK Trichem Co. Ltd., Korea*

5:36 PM — 6.2 – **Impact of Low-Frequency Phonons in High-k Gate Dielectric on Channel-Carrier Mobility of InGaZnO Thin-Film Transistor,** Q. H. Wang[1], H. Sun[1], Y. X. Ma[2], H. Su[1], and P. T. Lai[1], [1]*U. of Hong Kong, China,* [2]*Beijing Institute of Technology, China*

5:37 PM — 6.3 – **Enhancing Electrical Properties by Introducing Indium Oxide Buffer Layers to Control Interfacial Layer Formation between Metal Electrode and Insulator,** Y. A. Choi[1], S. Lee[1], J. H. Jeong[1], D. H. Kim[2], H. S. Oh[2], Y. J. Park[2], and W. J. Jeon[1], [1]*Kyung Hee U., Korea,* [2]*SK Trichem Co. Ltd., Korea*

5:38 PM — 6.4 – **Achieving High Current Density and 2DEG on Silicon thin-film Transistors via Sub-nanometer Thick PEALD $Ga_2O_3$ Polarization Modulation Layer,** B.-X. Wu, H.-L. Chuang, Z.-Y. Guo, W.-H. Chen, L.-C. Huang, and T.-H. Chang, *National Taiwan U., Taiwan*

5:39 PM — 6.5 – **Enhancing IWO TFT Reliability for M3D Integration with BEOL Compatible Encapsulation Layers,** J. Hartanto[1], B. Saini[1], D. Dede[1], Q. Lin[2], I. Radu[2], W. Tsai[1], and P. C. McIntyre[1], [1]*Stanford U.,* [2]*TSMC*

5:40 PM 6.6 – **Effect of $Si^+$ implantation and implant activation annealing in β-$Ga_2O_3$ MOS devices,** A. E. Islam[1], K. J. Liddy[1], W. Wang[2], A. Grilliot[2], M. Harrington[2], D. M. Dryden[1], K. D. Leedy[1], K. D. Chabak[1], and A. J. Green[1], [1]*Air Force Research Laboratory,* [2]*Wright State U.*

5:41 PM 6.7 – **Epitaxial Growth of β-$Ga_2O_3$ on MgO-buffered Si (100) substrates,** P. Espinosa Argaiz, A. B. Posadas, and A. A. Demkov, *UT Austin*

5:42 PM 6.8 – **A Fast Process for Vapor-deposited ZIF-8 MOF as low-k dielectrics and plasma etch selective seamless high aspect ratio and multiple aspect ratio gap fill,** D. Pal, N. Yang, and A. C. Kummel, *UCSD*

5:43 PM 6.9 – **Low Dielectric Constant $SiO_x$/$AlO_x$ Nanolaminate Film via Tuning the Si-to-Al Ratio,** X. Wang[1], J. Mu[1], J. Huang[1], Y. Cho[1], K. Wang[1], D. Pal[1], A. Yadav[2], K. Wong[2], E. Yieh[2], S. Nemani[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Applied Materials*

5:44 PM 6.10 – **Co metal ALD on Cu with Cyclic clean for Inverse Hybrid Metal Bonding,** C.-H. Kuo[1], J. Dutta[1], D. Pal[1], M. Manley[3], R. Sahay[3], R. Kanjolia[2], M. Moinpour[2], J. Woodruff[2], M. Bakir[3], and A. C. Kummel[1], [1]*UCSD,* [2]*EMD Performance Materials,* [3]*Georgia Tech*

5:45 PM 6.11 – **A Study on Electron Back-Scattered Diffraction Patterns for Inline Copper Treatment in Interconnect Fabrication,** J. Dutta, C.-H. Kuo, S. T. Ko, J. Luo, and A. C. Kummel, *UCSD*

5:46 PM 6.12 – **Next-Generation Interconnects: Developing Superior Interconnect Materials through Alloying Strategies and Combinatorial Co-Sputtering,** M. J. Kang and D. W. Lee, *Sungkyunkwan U., Korea*

5:47 PM 6.13 – **Saturation Dose Analysis of TiN Utilizing Titanium Tetrachloride and Hydrazine,** A. E. Ross[1], P. C. Lee[1], D. Pal[1], S. Yun[1], D. Go[1], J. Fammels[1], D. Mora[1], J. Spielman[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

5:48 PM 6.14 – **Controlling Chemisorption Behavior with Plasma Pre-treatment for Area Selective Deposition of Cobalt on TiN and Si Substrates in Interconnect Applications,** J. H. Park, Y. A. Choi, and W. J. Jeon, *Kyung Hee U., Korea*

5:49 PM 6.15 – **Combinatorial Investigation of Cu-Mn Alloy Thin Films as Interconnect Materials,** Y. I. Yun and D. W. Lee, *Sungkyunkwan U., Korea*

5:50 PM 6.16 – **Atomic Layer Annealing BN with Low Carbon Concentration,** P. C. Lee[1], D. Mora[1], D. Pal[1], A. E. Ross[1], J. Spielman[2], R. Kanjolia[3], M. Moinpour[3], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC,* [3]*EMD Performance Materials*

5:51 PM 6.17 – **High Quality AlN through Low-Pressure High-Power Impulse Magnetron Sputter Plus Kick,** P. C. Lee[1], D. Mora[1], D. Guo[1], S. Yun[1], M. Choi[2], S. Kumar[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Georgia Tech*

5:52 PM 6.18 – **Property Modulation of Aerosol Deposition AlN Using Multi-shot Laser Annealing for Gap Filling of Trench with Tens of μm Height,** D. Go[1], C. Meisner[1], V. Ashita[2], J. Garay[1], M. Bakir[2], and A. C. Kummel[1], [1]*UCSD,* [2]*Georgia Tech*

5:53 PM 6.19 – **Characterizing the Transport Properties and Trap States in Conformal Pt/$TiO_{2-x}$ Nanotube Diodes,** M. Michaels[1] and J. Kwon[2], [1]*Georgia Tech,* [2]*Infinity Power*

5:54 PM 6.20 – **Design of Optimized Silicon Avalanche Photodiodes with Desired Breakdown Voltage,** S. Ghazvini[1], G. Schuppener[2], W. Fan[2], S. Ramaswamy[2], and W. G. Vandenberghe[1], [1]*UT Dallas,* [2]*Texas Instruments Inc.*

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| 5:55 PM | 6.21 – **Hydrogen Gas Sensor Based on the Electrospun $SnO_2$ Nanofibers with Electrospinning Time,** H. Yoon, S. Lee, J. Kim, S. Kim, Y. Jeon, J. Ryu, M. Kwon, K. Na, and W. Choi, *Gangneung-Wonju National U., Korea* |
| 6:00 PM | Adjourn |
| 7:00 PM–10:00 PM | Reception/Poster Session |

# Friday, December 13, 2024

## Session 7: Ferroelectrics II

Session Chair: TBD

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|---|---|
| 8:30 AM | 7.1 *Invited* – **Hafnia-Based FeRAM for High-Density, High-Speed Embedded Memory,** C. Neumann, *Intel* |
| 9:00 AM | 7.2 – **Unveiling Hole Trap Behaviors in Program and Erase Operations of Silicon-based FeFETs: Experimental Insights, Simulations, and Deep Understanding,** L. Jiao, Z. Zhou, X. Wang, Z. Zheng, and X. Gong, *National U. of Singapore, Singapore* |
| 9:20 AM | 7.3 – **Strategies for Reducing Interface and Bulk Traps of FeFETs to Improve Endurance: Insights from Charge Pumping Measurements,** M. R. Sk[1], S. Roy[1], Y. Raffel[2], M. Lederer[2], K. Seidel[2], S. De[3], and B. Chakrabarti[1], [1]*IIT Madras, India,* [2]*Fraunhofer IPMS-CNT, Germany,* [3]*National Tsing Hua U., Taiwan* |
| 9:40 AM | 7.4 – **In-Memory Computing via Cross-Point Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Capacitors Driven by Remanent Polarization,** M. Lee, J.-H. Kim, and J. Kim, *UT Dallas* |
| 10:00 AM | 7.5 – **Quantitative Analysis of Intrinsic Trap Density in α-$In_2Se_3$ FeS-FETs by De-Embedding Parasitic Capacitance Using Modified Conductance Method,** M. Park[1], J. Yoo[1], H. Lee[1], H. Song[1], S. Kim[1], S. Lim[1], S. Park[1], S. Jung[1], K. Heo[1], T. Kim[3], P. D. Ye[2], and H. Bae[1], [1]*Jeonbuk National U., Korea,* [2]*Purdue U.,* [3]*U. of Seoul, Korea* |
| 10:20 AM | 7.6 – **Plasma-Enhanced Atomic Layer Deposition of Wurtzite AlN-Based Ferroelectrics,** D. A. Dalba[1], S. Saadat Niavol[1], X. Zhang[2], W. Xu[2], B. Bhattarai[1], D. M. Gamachchi[1], I. M. Karunarathne[1], D. Cao[2], W. J. Meng[2], and A. C. Meng[1], [1]*U. of Missouri,* [2]*Louisiana State U.* |
| 10:40 AM | Coffee break |

## Session 8: Advanced Logic I

Session Chair: TBD

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| 10:55 AM | 8.1 *Invited* – **CFET Technology for Future Logic Scaling,** S. Liao, *TSMC* |
| 11:25 AM | 8.2 – **Accurate Extraction of Donor- and Acceptor-like Interface Trap Density by Photonic GIDL Characteristics in Vertically Stacked Si-NW GAA FETs,** S. Park[1], J. Yoo[1], H. Lee[1], H. Song[1], S. Kim[1], S. Lim[1], M. Park[1], S. Jung[1], T. Kim[3], Y.-K. Choi[2], and H. Bae[1], [1]*Jeonbuk National U., Korea,* [2]*KAIST, Korea,* [3]*U. of Seoul, Korea* |
| 11:45 AM | 8.3 – **Improved Electrical Characteristics of Ge FinFET CMOS Invertor with Low Power Rapid Plasma Oxidation Treatment,** H.-C. Yang[1], D.-B. Ruan[2], K.-S. Chang-Liao[1], and C.-H. Li[1], [1]*National Tsing Hua U., Taiwan,* [2]*Fuzhou U., China* |

12:05 PM Adjourn for lunch

12:10 PM–1:55 PM Committee/Invited speaker luncheon (by invitation only)

## Session 9: Advanced Logic II

Session Chair: TBD

2:00 PM 9.1 *Invited* – **Gate Stack Innovations for Gate-All-Around (GAA) Device Architecture to Continue Transistor Scaling,** R. Bao, *IBM*

2:30 PM 9.2 – **The localized interface/channel states in Gate-All-Around transistors (GAAFETs): physical origins and distribution,** Y.-Y. Liu[1], R. Wang[2], and X. Jiang[3], [1]*Chinese Academy of Sciences, China,* [2]*Peking U., China,* [3]*National Natural Science Foundation of China, China*

2:50 PM 9.3 – **Enhanced Breakdown Voltage and Photo Response of Ultrathin Body Nanosheets,** B.-W. Huang, W.-J. Chen, Y.-R. Chen, and C. W. Liu, *National Taiwan U., Taiwan*

3:10 PM 9.4 – **Density Functional Analysis of Threshold Voltage Control in High K Gate Stacks,** R. Cao[1,3], H. Guo[2], Y. Guo[2], J. W. Luo[3], and J. Robertson[1], [1]*Cambridge U., UK,* [2]*Wuhan U., China,* [3]*Chinese Academy of Sciences, China*

3:30 PM Coffee break

## Session 10: Defects

Session Chair: J. Franco

3:45 PM Limerick contest introduction

3:50 PM 10.1 *Honorary lecture* – **Electron Spin Resonance as Powerful Spectroscopy for Assessment of Point Defects in Semiconductor/Insulator Structures: Some Historical Reflections on Interfaces,** A. Stesmans, *U. Leuven, Belgium*

4:25 PM 10.2 – **Physical modeling of the Interface States of FinFET at Cryogenic Temperature,** Z. Wang[1], H. Wang[2], W. Li[3], Y. Wang[2], L. Zeng[2], Y.-Y. Liu[3], and R. Wang[1], [1]*Peking U., China,* [2]*Beihang U., China,* [3]*Chinese Academy of Sciences, China*

4:45 PM 10.3 – **Generation of the Interface-Originated Band-Edge States by Hot Carrier Degradation Increasing Threshold Voltage at Cryogenic Temperatures,** S. Shitakata[1,2], H. Oka[1], K. Kato[1], T. Inaba[1], S. Iizuka[1], H. Asai[1], and T. Mori[1], [1]*AIST, Japan,* [2]*Keio U., Japan*

5:05 PM 10.4 – **Unveiling the Influence of Defects on Dielectric Lifetimes Using Low-Frequency Noise,** N. Saini[1,2], D. Tierno[1], K. Croes[1], V. V. Afanas'ev[1,2], and J. Van Houdt[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

5:25 PM 10.5 – **Role of electron and hole trapping in amorphous oxides in defect generation,** C. Kaewmeechai, T. Cobos Freire, J. Strand, and A. Shluger, *UCL, UK*

5:45 PM Adjourn

7:00 PM–10:00 PM Conference Banquet & Limerick Contest

# Saturday, December 14, 2024

## Session 11: Emerging Memory

Session Chair: TBD

8:30 AM — 11.1 *Invited* – **Pioneering Innovation for Next Generation 3D Memory Era,** K. Park, *Samsung*

9:00 AM — 11.2 – **A One-Transistor DRAM Memory Cell Utilizing $HfO_2$-Based Ferroelectric Polarization-Assisted Charge-Trapping,** M. K. Bai[1,2], X. Q. Sun[1,2], R. Han[1,2], T. Hu[1,2], J. S. Chai[1,2], H. Xu[1,2], X. Wang[1,2], W. W. Wang[1,2], and T. Ye[1,2], [1]*Chinese Academy of Sciences, China,* [2]*U. of Chinese Academy of Sciences, China*

9:20 AM — 11.3 – **Optimization of IGZO-Channel FeFETs: Enhancing Memory Window and Endurance through Channel Thickness and Area Scaling,** Z. Chen[1,2], N. Ronchi[1], W. Zheng[1], H.-C. Kim[1,2], R. Izmailov[1,2], B. Truijen[1], S. Subhechha[1], S. Van Beek[1], A. M. Walke[1], A. Chasin[1], M. I. Popovici[1], J. Li[1], H. Tang[1,2], G. Van den Bosch[1], M. Rosmeulen[1], V. V. Afanas'ev[1,2], and J. Van Houdt[1,2], [1]*imec, Belgium,* [2]*U. Leuven, Belgium*

9:40 AM — 11.4 – **Nonvolatile Memory and Artificial Synapse Characteristics of Electrochemical Random-Access Memory with Atomic Layer Deposited ZnO and $HfO_{2-x}$ Layers through Oxygen Ion-Exchange,** J. Han, J. Ryu, T. Noh, J.-G. Park, P. H. Chung, and T.-S. Yoon, *Ulsan National Institute of Science and Technology, Korea*

10:00 AM — Coffee break

## Session 12: Wide Bandgap Semiconductors

Session Chair: TBD

10:15 AM — 12.1 *Invited* – **Device Engineering for High-Performance Gallium Oxide Electronics,** S. Rajan, *Ohio State U.*

10:45 AM — 12.2 – **β-$Ga_2O_3$-on-SiC RF MOSFETs,** M. Zhou, H. Zhou, J. Zhang, and Y. Hao, *Xidian U., China*

11:05 AM — 12.3 – **Characteristics of beta-$Ga_2O_3$/$Al_2O_3$/Pt capacitors with modified $Ga_2O_3$ surface using dummy $SiO_2$ technique,** T. Nabatame, Y. Irokawa, T. Sawada, M. Miyamoto, H. Miura, Y. Koide, and K. Tsukagoshi, *NIMS, Japan*

11:25 AM — 12.4 – **Reversible Polarity of GaN / Si Surfaces Using Low Energy Ions During ALD,** S. Yun[1], P. C. Lee[1], J. Spielman[2], and A. C. Kummel[1], [1]*UCSD,* [2]*RASIRC*

11:45 AM — 12.5 – **DFT study on electronic structure and carrier scattering property at 4H-SiC/$SiO_2$ after NO annealing,** T. Ono, M. Uemoto, N. Funaki, and K. Sugiyama, *Kobe U., Japan*

12:05 PM — Conference closing remarks

# Author Index

# Affiliation Index