

SISC 2009

**40th IEEE
Semiconductor Interface
Specialists Conference**

December 3-5, 2009 (Tutorial: Dec 2)
Key Bridge Marriott Hotel, Arlington, VA
www.ieeesisc.org



FINAL PROGRAM

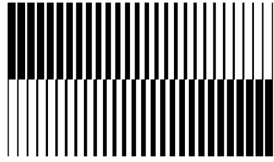
General Chair: Dina Triyoso

Technical Chair: Martin M. Frank

Arrangements Chair: John Robertson

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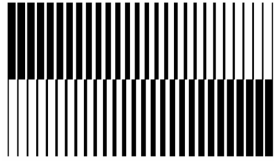
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SISC Ed Nicollian Award for Best Student Paper

In 1995, the SISC began presenting an award for the best student presentation, in honor of Professor E.H. Nicollian, University of North Carolina at Charlotte. Professor Nicollian was a pioneer in the exploration of the metal-oxide-semiconductor system, particularly in the area of electrical measurements. His efforts were fundamental in establishing the SISC in its early years, and he served as its technical program chair in 1982. With John Brews, he wrote the definitive book, “MOS Physics and Technology,” published by Wiley Interscience.

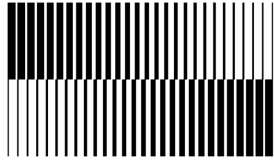
The *SISC Ed Nicollian Award for Best Student Paper* is presented to the lead student author or either an oral or poster presentation. The winner is chosen by members of the technical program committee at the end of the SISC. The award consists of a plaque, an honorarium, and a permanent mention on the conference web site.

Winner of the 2008 SISC Ed Nicollian Award for Best Student Paper:

Marko Milojevic, *University of Texas at Dallas*

“In-situ XPS investigation of the ‘clean-up’ effect
through half-cycle ALD reactions on III-V substrates”

with B. Brennan, F.S. Aguirre-Tostado, C.L. Hinkle, H.C. Kim, B. Lee, G.J. Hughes, E.M. Vogel,
J. Kim, and R.M. Wallace



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Wednesday Evening Tutorial

Wednesday, December 2, 2009, 8:00 PM

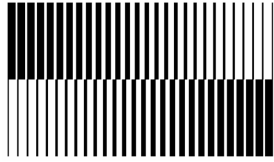
First introduced at SISC 2008, the Wednesday evening Tutorial aims to provide a good foundation in a topic frequently covered at the conference, particularly benefiting students and newcomers to the field. The Tutorial is free to all registered SISC attendees.

Dr. Thomas Schroeder

IHP, Frankfurt (Oder), Germany

**“Physical Characterization of thin oxide films by XRD and XPS:
From conventional laboratory to modern synchrotron techniques”**

The integration of nano-scaled oxide layers (e.g. gate dielectrics for CMOS, ferroelectrics and resistive switching oxides for non-volatile memories etc.) in Si technologies requires strict thin film deposition control to gain maximum performance and reliability. X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) are well-established laboratory techniques to generally gain in a non-destructive way information about the key parameters structure and stoichiometry, respectively. After a brief introduction into the basic physics of these methods, the tutorial will focus on innovative synchrotron based XRD and XPS methods to overcome experimental limits still existing with laboratory equipment. Special emphasis will be placed in the structure part on X-ray standing wave techniques to learn about the atomic configuration of the oxygen sublattice (difficult to detect by conventional XRD) and in the stoichiometry part on high-energy XPS techniques to unveil the characteristics of buried films and interfaces (impossible to access by standard XPS).



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Conference Agenda Overview

Wednesday, December 2, 2009

Registration	6:00 PM – 8:00 PM
Hospitality Room	8:00 PM – Midnight
Evening Tutorial	8:00 PM – 9:30 PM

Thursday, December 3, 2009

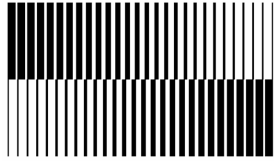
Registration	8:00 AM – 5:00 PM
Session 1 – High-k Gate Stacks I	8:00 AM – 9:10 AM
Poster Session 1 – Oxides on Si and SiGe, Memory	9:15 AM – 9:48 AM
Session 2 – Oxide Electronics	10:20 AM – 11:20 AM
Poster Session 2 – Oxide Electronics and III-V Semiconductors	11:25 AM – 11:49 AM
Session 3 – The 40th SISC: Special Invited Talk	1:30 PM – 2:20 PM
Poster Session 3 – Reliability and Electrical Characterization	2:25 PM – 2:49 PM
Session 4 – III-V Semiconductors and Germanium	3:20 PM – 5:00 PM
Poster Session 4 – Germanium	5:05 PM – 5:29 PM
Poster Reception	7:00 PM – 10:00 PM
Hospitality Room	9:30 PM – Midnight

Friday, December 4, 2009

Registration	8:00 AM – Noon
Session 5 – III-V Semiconductors	8:00 AM – 10:00 AM
Session 6 – Memory Technology	10:30 AM – 11:50 PM
Session 7 – Graphene	11:50 AM – 12:35 PM
Technical Committee / Invited Speaker Luncheon	12:40 PM – 2:00 PM
Rump Session	3:00 PM – 5:30 PM
Conference Banquet and Limerick Contest	7:00 PM – 10:00 PM
Hospitality Room	10:00 PM – Midnight

Saturday, December 5, 2009

Session 8 – Reliability and Interface Defects	8:30 AM – 10:10 AM
Session 9 – High-k Gate Stacks II	10:40 AM – 12:25 PM



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Conference Program

Session 1 – High-k Gate Stacks I

Thursday, December 3, 2009

Session Chair: D. Triyoso

8:00 AM Welcome and opening remarks

8:15 AM 1.1 *Invited* - **Quality control of high-k gate oxides by doping with impurities: Guidelines from theoretical analysis**, N. Umezawa, *National Institute for Materials Science (NIMS), Japan*

8:50 AM 1.2 - **Threshold adjustment of nitride-gated pFETs**, M. Copel, E. Cartier, M. Hopstaken, *IBM*

Poster Session 1 – Oxides on Si and SiGe, Memory

Thursday, December 3, 2009

Session Chair: C. Young

9:15 AM P.1 - **The Plasma Nitridation and Post Annealing Effects on HfLaO Gate Dielectrics**, K. Ariyoshi¹, L.F. Edge², T. Vo², J. Bruley², L. Tai², R. Iijima¹, Y. Tsuchiya¹, M. Takayanagi¹, V. Paruchuri², ¹*Toshiba America Electronic Components*, ²*IBM*

9:18 AM P.2 - **Intrinsic Defect Levels in Al₂O₃**, D. Liu¹, S.J. Clark², J. Robertson¹, ¹*Cambridge University, UK*, ²*Durham University, UK*

9:21 AM P.3 - **Effect of oxygen vacancies and interfacial oxygen concentration on local structure and band offsets in a model metal-HfO₂-SiO₂-Si gate stack**, E. Cockayne¹, B. Magyari-Kope², Y. Nishi², ¹*National Institute of Standards and Technology (NIST)*, ²*Stanford University*

9:24 AM P.4 - **Effect of thickness of the chemical oxide interfacial layer on the interfacial quality of HfO₂ on silicon**, Z. Chen, S. Li, *University of Kentucky*

9:27 AM P.5 - **Gentle Gate Last Process Integration and Electrical Characterization of TiN/Gd₂O₃/Si MOS Capacitors and Field Effect Transistors**, R. Endres, T. Krauss, F. Wessely, U. Schwalke, *Darmstadt University of Technology, Germany*

9:30 AM P.6 - **Electronic properties of Ge dangling bonds at (100)Si_{1-x}Ge_x/SiO₂ interfaces: A first-principles study**, M. Houssa¹, G. Pourtois², V.V. Afanas'ev¹, A. Stesmans¹, M.M. Heyns², ¹*University of Leuven, Belgium*, ²*IMEC, Belgium*

9:33 AM P.7 - **Direct Extraction of Mobility and Effective Carrier Velocity in SiGe Short Channel pMOSFET Using RF C-V Measurement**, K.T. Lee¹, G.-B. Choi¹, H.C. Sagong¹, M.-S. Park¹, C.Y. Kang², H.-H. Tseng², R. Jammy², J.-S. Lee¹, Y.-H. Jeong¹, ¹*Pohang University of Science and Technology (POSTECH), Korea*, ²*SEMATECH*

9:36 AM P.8 - **Tailoring lattice parameters & band gaps with thin crystalline mixed oxide buffer layers on Si: The example of lattice matched epi-Si(111)/PrYO₃/Si(111) heterostructures**, O. Seifarth, A. Giussani, P. Zaumseil, T. Schroeder, *IHP, Germany*

9:39 AM P.9 - **Tayloring the Si₃N₄/Al₂O₃ interface in TANOS non-volatile memory stack fabrication**, M. Czernohorsky¹, T. Melde¹, P.P. Michalowski¹, J. Paul¹, A.T. Tilke², M.F. Beug², V. Beyer¹, ¹*Fraunhofer Center Nanoelectronic Technologies (CNT), Germany*, ²*Qimonda, Germany*

9:42 AM P.10 - **Charge trapping effects on memory windows in SOI FinFET ZRAM transistors**, E. Zhang¹, D.M. Fleetwood¹, F.E. Mamouni¹, D.R. Balla¹, M.L. Alles¹, R.D. Schrimpf¹, W. Xiong², S. Cristoloveanu³, ¹*Vanderbilt University*, ²*Texas Instruments*, ³*IMEP, Grenoble INP, MINATEC, France*

9:45 AM P.11 - **Effect of Filament Resistance on Retention Characteristics of ReRAM**, J. Park, J. Yoon, M. Jo, D. Seong, J. Lee, W. Lee, J. Shin, E.M. Bourim, H. Hwang, *Gwangju Institute of Science and Technology (GIST), Korea*

9:48 AM Break

Session 2 – Oxide Electronics

Thursday, December 3, 2009

Session Chair: K. Shiraishi

10:20 AM Opening remarks

10:25 AM 2.1 *Invited* - **Novel charge-based multiferroic composite heterostructures**, C.A.F. Vaz, J. Hoffman, C.H. Ahn, *Yale University*

11:00 AM 2.2 - **Role of surface water in the reversible metal-insulator transition at the LaAlO₃/SrTiO₃ interface**, C.S. Hellberg¹, K.E. Andersen², ¹*Naval Research Lab*, ²*High Performance Technologies, Inc., Naval Research Lab*

Poster Session 2 – Oxide Electronics and III-V Semiconductors

Thursday, December 3, 2009

Session Chair: A. Stesmans

11:25 AM P.12 - **Metal-Insulator Transitions in Strongly Correlated Oxides: A novel paradigm for ultra-fast electronics**, C. Ko, S. Ramanathan, *Harvard University*

11:28 AM P.13 - **Ultra-shallow doping for V_T adjustment in deep submicron InGaAs MOSFET by sulfur monolayer**, Y.Q. Wu, J.J. Gu, P.D. Ye, *Purdue University*

11:31 AM P.14 - **Susceptibility of InGaAs MISFETs to Thermal Processes in the Device Fabrication**, T. Yasuda¹, H. Ishii¹, Y. Urabe¹, T. Itatani¹, N. Miyata¹, H. Yamada², N. Fukuhara², M. Hata², M. Yokoyama³, M. Takenaka³, S. Takagi³, ¹National Institute of Advanced Industrial Science and Technology (AIST), Japan, ²Sumitomo Chemical, Japan, ³The University of Tokyo, Japan

11:34 AM P.15 - **Interface State Response in HfO₂ Gated Strained InAs Quantum Well FETs**, H. Madan¹, A. Ali¹, S. Koveshnikov², S. Datta¹, ¹Pennsylvania State University, ²SUNY Albany

11:37 AM P.16 - **Investigation of Forming Gas Annealing of High-k/p-In_{0.53}Ga_{0.47}As/InP Metal-Oxide-Semiconductor Capacitors**, R.D. Long^{1,2}, B. Shin², R.E. Nagle¹, K. Cherkaoui¹, J. Cagnon³, S. Stemmer³, S. Monaghan¹, A. O' Mahony¹, I. Povey¹, M.E. Pemble¹, P.C. McIntyre², P.K. Hurley¹, ¹Tyndall National Institute, University College Cork, Ireland, ²Stanford University, ³UC Santa Barbara

11:40 AM P.17 - **In situ-MEIS, XPS, and C-V investigation of native oxide reduction on GaAs during atomic layer deposition**, H.D. Lee, T. Feng, L. Yu, D. Mastrogiovanni, A. Wan, E. Garfunkel, T. Gustafsson, *Rutgers University*

11:43 AM P.18 - **GaSb - An Unexplored III-V Channel Material for PMOSFET**, M. Xu, R. Wang, P.D. Ye, *Purdue University*

11:46 AM P.19 - **Impact of Forming Gas Annealing on the Electrical Characterization of ALD Al₂O₃/In_{0.53}Ga_{0.47}As MOS Capacitors**, J. Hu, H.-S.P. Wong, *Stanford University*

11:49 AM Adjourn for lunch

Session 3 – The 40th SISC: Special Invited Talk

Thursday, December 3, 2009

Session Chair: M.M. Frank

1:30 PM Opening remarks

1:35 PM 3.1 *Invited* - **Gate Dielectrics, Interfaces, and SISC**, T.P. Ma, *Yale University*

Poster Session 3 – Reliability and Electrical Characterization

Thursday, December 3, 2009

Session Chair: D. Ielmini

2:25 PM P.20 - **Investigation of SILC via Energy Resolved Spin Dependent Tunneling Spectroscopy**, J.T. Ryan¹, P.M. Lenahan¹, A.T. Krishnan², S. Krishnan², ¹Pennsylvania State University, ²Texas Instruments

2:28 PM P.21 - **Characterization of fast charge trapping sources in bias temperature instability in high-k MOSFET**, M. Jo¹, M. Chang¹, S. Kim¹, S. Jung¹, J.-B. Park¹, H.-S. Jung², R. Choi³, H. Hwang¹, ¹Gwangju Institute of Science and Technology (GIST), Korea, ²Samsung Electronics, Korea, ³Inha University, Korea

2:31 PM P.22 - **Stress polarity in bias-temperature instability on MOSFETs with HfO₂/LaO_x and HfO₂/AlO_x dielectric stacks**, C.-C. Lu, K.-S. Chang-Liao, Y.-F. Cheng, C.-H. Tsao, T.-K. Wang, *National Tsing Hua University, Taiwan*

2:34 PM P.23 - **What Triggers NBTI? An "On The Fly" Electron Spin Resonance Approach**, J.T. Ryan¹, P.M. Lenahan¹, T. Grasser², H. Enichlmair³, ¹*Pennsylvania State University*, ²*Technical University of Vienna, Austria*, ³*austriamicrosystems, Austria*

2:37 PM P.24 - **Hot Carrier Induced Degradation in Aggressively Scaled ($L_{\text{gate}} = 25$ nm) high-k/metal gate FINFETs**, M. Wang¹, K. Maitra², H. Jagannathan¹, V.S. Basker¹, H. Bu¹, V. Paruchuri¹, B. Doris¹, J.H. Stathis¹, ¹*IBM*, ²*GLOBALFOUNDRIES*

2:40 PM P.25 - **Comparison of Reliability Properties in SiGe/Si and Si Channel High-k/Metal Gate Stacks pMOSFETs**, M.S. Park^{1,2,4}, K.T. Lee^{1,2,4}, C.Y. Kang¹, B.-G. Min⁵, J. Oh¹, P. Majhi¹, H.-H. Tseng¹, J.C. Lee⁴, J.-S. Lee², R. Jammy¹, Y.-H. Jeong^{2,3}, ¹*SEMATECH*, ²*Pohang University of Science and Technology (POSTECH), Korea*, ³*National Center for Nanomaterials Technology (NCNT), Korea*, ⁴*The University of Texas at Austin*, ⁵*Jusung Engineering, Korea*

2:43 PM P.26 - **Impact of Hole Non Parabolicity on EOT extraction from CV measurements**, J. Coignus^{1,2}, R. Clerc¹, C. Leroux², G. Ghibaudo¹, G. Reimbold², F. Boulanger², ¹*IMEP-LAHC/MINATEC-INPG, France*, ²*CEA-LETI/MINATEC, France*

2:46 PM P.27 - **Demonstration of a Wafer-level Hall-Mobility Measurement Technique**, L.C. Yu^{1,2}, K.P. Cheung¹, V. Tilak³, G. Dunne³, K. Matocha³, J.P. Campbell¹, J.S. Suehle¹, K. Sheng², ¹*National Institute of Standards and Technology (NIST)*, ²*Rutgers University*, ³*GE Global Research*

2:49 PM Break

Session 4 – III-V Semiconductors and Germanium

Thursday, December 3, 2009

Session Chair: M. Houssa

3:20 PM Opening remarks

3:25 PM 4.1 *Invited* - **Passivation of InGaAs and InAs by ALD Precursors**, J.B. Clemens¹, E.A. Chagarov¹, M. Holland², R. Droopad³, J. Shen¹, A.C. Kummel¹, ¹*UC San Diego*, ²*University of Glasgow, UK*, ³*Texas State University - San Marcos*

4:00 PM 4.2 - **New Insights into Flatband Voltage Shift and Minority Carrier Generation in GeO₂/Ge MOS devices**, T. Hosoi¹, M. Saito¹, I. Hideshima¹, G. Okamoto¹, K. Kutsuki¹, S. Ogawa², T. Yamamoto^{1,2}, T. Shimura¹, H. Watanabe¹, ¹*Osaka University, Japan*, ²*Toray Research Center, Japan*

4:20 PM 4.3 - **Interface Passivation Analysis of Ge/GeO₂ pMOS and nMOS With and Without Forming Gas Anneal**, K. Martens¹, F. Bellenger^{1,2}, A. Delabie¹, B. De Jaeger¹, M. Meuris¹, G. Groeseneken^{1,2}, ¹*IMEC, Belgium*, ²*University of Leuven, Belgium*

4:40 PM 4.4 - **Kinetic Study of GeO Desorption from Ge/GeO₂ system**, S.K. Wang¹, K. Kita^{1,2}, C.H. Lee¹, T. Tabata^{1,2}, K. Nagashio^{1,2}, T. Nishimura^{1,2}, A. Toriumi^{1,2}, ¹*The University of Tokyo, Japan*, ²*JST-CREST, Japan*

Poster Session 4 – Germanium

Thursday, December 3, 2009

Session Chair: P.D. Ye

5:05 PM P.28 - **Sub-gap Formation and Its Annihilation in Energy Band Gap of GeO₂ by Changing O₂ Pressure in PDA Process**, M. Yoshida¹, K. Kita^{1,2}, K. Nagashio^{1,2}, T. Nishimura^{1,2}, A. Toriumi^{1,2}, ¹*The University of Tokyo, Japan*, ²*JST-CREST, Japan*

5:08 PM P.29 - **Characterization of the "clean-up" of the GeO and GeON passivated Ge(100) surfaces by ALD using in-situ monochromatic XPS**, M. Milojevic¹, R. Contreras-Guerrero², M. Lopez-Lopez², J. Kim¹, R. M. Wallace¹, ¹*University of Texas at Dallas*, ²*CINVESTAV-Unidad Zacatenco, Mexico*

5:11 PM P.30 - **Impact of plasma nitridation of thermally-grown GeO₂/Ge MIS structures on the GeO₂ film and interface properties**, T. Iwasaki¹, N. Taoka², M. Takenaka¹, S. Takagi¹, ¹*The University of Tokyo, Japan*, ²*National Institute of Advanced Industrial Science and Technology (AIST), Japan*

5:14 PM P.31 - **Passivation of Ge(100) Surface studied by Scanning Tunneling Microscopy and Density Functional Theory**, J.S. Lee, S.R. Bishop, A.C. Kummel, *UC San Diego*

5:17 PM P.32 - **Electrical and interfacial properties of LaLuO₃ and GdScO₃ ternary oxides for Ge CMOS applications**, J.M.J. Lopes^{1,2}, M. Roeckerath^{1,2}, E. Durgun-Ozben^{1,2}, A. Nichau^{1,2}, G. Mussler^{1,2}, C. Radtke³, G.G. Marmitt³, C. Krug³, G.V. Soares³, I.J.R. Baumvol³, J. Schubert^{1,2}, S. Mantl^{1,2}, ¹*Research Center Juelich, Germany*, ²*JARA, Germany*, ³*UFRGS, Brazil*

5:20 PM P.33 - **Charge Pumping Study of the Trap Density in CF₄ treated TiN/Ga₂O₃(Gd₂O₃)/Ge**, C.A. Lin, L.K. Chu, T.D. Lin, R.L. Chu, L.T. Tung, M. Hong, J. Kwo, *National Tsing Hua University, Taiwan*

5:23 PM P.34 - **Trigonal interface defect in epi-Ge₃N₄/(111)Ge observed by electron spin resonance**, A. Stesmans, A.P.D. Nguyen, V.V. Afanas'ev, *University of Leuven, Belgium*

5:26 PM P.35 - **Local GeO₂ Doping at LaLuO₃/Ge Interface for Direct High-k/Ge Gate Stacks**, T. Tabata^{1,2}, C.H. Lee¹, K. Kita^{1,2}, A. Toriumi^{1,2}, ¹*The University of Tokyo, Japan*, ²*JST-CREST, Japan*

5:29 PM Adjourn

7:00 PM Poster Reception

Session 5 – III-V Semiconductors

Friday, December 4, 2009

Session Chair: R. Wallace

8:00 AM Morning announcements

8:05 AM 5.1 *Invited* - **Fermi level pinning and its removal at III-V MOS interfaces**, H. Hasegawa, M. Akazawa, *Hokkaido University, Japan*

8:40 AM 5.2 - **Inelastic Electron Tunneling Spectroscopy study of ultra-thin TiO₂/Al₂O₃ on GaAs**, Z. Liu¹, S. Cui¹, W. Zhang¹, Y. Yang¹, T.P. Ma¹, ¹*Yale University*

9:00 AM 5.3 - **Impact of InGaAs Surface Nitridation on Interface Properties of InGaAs MOS Capacitors using Electron Cyclotron Resonance Plasma Sputtering SiO₂**, T. Hoshii¹, M. Yokoyama¹, H. Yamada², M. Hata², T. Yasuda³, M. Takenaka¹, S. Takagi¹, ¹*The University of Tokyo, Japan*, ²*Sumitomo Chemical, Japan*, ³*National Institute of Advanced Industrial Science and Technology (AIST), Japan*

9:20 AM 5.4 - **Impact of Interface States on Sub-threshold Response of III-V MOSFETs, MOS HEMTs and Tunnel FETs**, W.C. Kao, E. Hwang, S. Mookerjee, S. Datta, *Pennsylvania State University*

9:40 AM 5.5 - **Schottky-Barrier Modulation of Metal/In_{0.53}Ga_{0.47}As Interface with ALD Ultra-thin Al₂O₃ Passivation**, R. Wang^{1,2}, M. Xu¹, P.D. Ye¹, R. Huang², ¹*Purdue University*, ²*Peking University, China*

10:00 AM Break

Session 6 – Memory Technology

Friday, December 4, 2009

Session Chair: H. Hwang

10:30 AM Opening remarks

10:35 AM 6.1 *Invited* - **Memory technology: Evolutionary versus revolutionary concepts**, J. Van Houdt, *IMEC, Belgium*

11:10 AM 6.2 - **Physical & Electrical Characterization of Fluorine Passivation for Improving Band-Engineered SiO₂/HfSiO/SiO₂ (OHO) TANOS Flash Memory**, S. Verma^{1,2}, D.C. Gilmer¹, P. Lysaght¹, J. Price¹, G. Bersuker¹, P.D. Kirsch¹, H.-H. Tseng¹, R. Jammy¹, K.C. Saraswat², ¹*SEMATECH*, ²*Stanford University*

11:30 AM 6.3 - **Read-disturb limited reliability of multilevel NiO-based resistive-switching memory**, D. Ielmini¹, F. Nardi¹, A. Vigani¹, E. Cianci², S. Spiga², ¹*Politecnico di Milano and IUNET, Italy*, ²*Laboratorio Nazionale MDM, CNR-INFN, Italy*

Session 7 – Graphene

Friday, December 4, 2009

Session Chair: M. Fischetti

11:50 AM Opening remarks

11:55 AM 7.1 - **ALD high-k dielectric integration on epitaxial graphene by inserting 1 nm fully oxidized aluminum as seeding layer**, J.J. Gu¹, T. Shen², Y.Q. Wu¹, M. Bolen¹, M. Capano¹, P.D. Ye¹, *Purdue University*

12:15 AM 7.2 - **Metal dependent contact properties in graphene FETs**, K. Nagashio, T. Nishimura, K. Kita, A. Toriumi, *The University of Tokyo, Japan*

12:35 PM Adjourn for lunch – Technical Committee and Invited Speaker Luncheon

3:00 PM Rump Session - **Graphene: Vision – and reality?** with an introductory statement by A. Toriumi, *The University of Tokyo, Japan*

7:00 PM Conference Banquet and Limerick Contest

Session 8 – Reliability and Interface Defects

Saturday, December 5, 2009

Session Chair: K. Maitra

8:30 AM Morning Announcements

8:35 AM 8.1 *Invited* - **How to improve mobility, performance, and BTI reliability of high-k/metal gate transistors?**, X. Garros, M. Cassé, G. Reimbold, F. Martin, F. Boulanger, *CEA-LETI/MINATEC, France*

9:10 AM 8.2 - **Impact of Si-Passivation Thickness and Processing on NBTI Reliability of Ge and SiGe pMOSFETs**, J. Franco^{1,2}, B. Kaczer¹, A. Stesmans², V.V. Afanas'ev², K. Martens¹, M. Aoulaiche¹, T. Grasser³, J. Mitard¹, G. Groeseneken^{1,2}, ¹*IMEC, Belgium*, ²*University of Leuven, Belgium*, ³*Technical University of Vienna, Austria*

9:30 AM 8.3 - **Electronic properties of Ge dangling bond centres at Si_{1-x}Ge_x/SiO₂ interfaces**, V.V. Afanas'ev, M. Houssa, A. Stesmans, *University of Leuven, Belgium*

9:50 AM 8.4 - **Oxidizing and Nitriding Reactions Originated with Nitrogen Released from TiN in Poly-Si/TiN/HfO₂/SiO₂ Gate Stack**, T. Matsuki¹, K. Ohmori², T. Morooka¹, T. Suzuki¹, M. Sato¹, K. Kimoto³, T. Nabatame³, S. Miyazaki⁴, K. Shiraishi⁵, T. Chikyow³, K. Yamada², J. Yugami¹, Y. Matsui³, K. Ikeda¹, Y. Ohji¹, ¹*Semiconductor Leading Edge Technologies (Selete), Japan*, ²*Waseda University, Japan*, ³*National Institute for Materials Science (NIMS), Japan*, ⁴*Hiroshima University, Japan*, ⁵*University of Tsukuba, Japan*

10:10 AM Break

Session 9 – High-k Gate Stacks II

Saturday, December 5, 2009

Session Chair: J. Schaeffer

10:40 AM Opening remarks

10:45 AM 9.1 - **The germanium surface and the effect of La chemistry on the Ge surface passivation**, A. Dimoulas, Y. Panayiotatos, D. Tsoutsou, S.F. Galata, G. Mavrou, A. Sotiropoulos, *NCSR DEMOKRITOS, Greece*

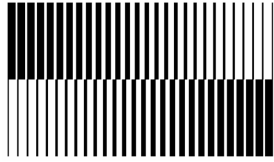
11:05 AM 9.2 - **Effective Work Function Control of TaC/High-k Gate Stack by Post Metal Nitridation**, T. Ando^{1,2}, A. Callegari¹, C. Choi¹, M. Hopstaken¹, J. Bruley¹, M. Gordon¹, H. Watanabe², V. Narayanan¹, ¹*IBM*, ²*Osaka University, Japan*

11:25 AM 9.3 - **Atomic mechanism of Flat-band Voltage shifts by La, Sr, Al and Nb induced Dipole Layers**, L. Lin, J. Robertson, *Cambridge University, UK*

11:45 AM 9.4 - **XPS Analysis of High-k/SiO₂/Si Stacks through Grounded Gate Metal - Estimation of Energy Levels of Electronic Structures of High-k Dielectric Films**, Y. Chikata, K. Kita, T. Nishimura, K. Nagashio, A. Toriumi, *The University of Tokyo, Japan*

12:05 AM 9.5 - **Crystalline Lattice-Matched Ba_{0.7}Sr_{0.3}O on Si(001) as Gate Dielectric**, K.R. Hofmann, A. Cosceev, D. Müller-Sajak, H. Pfnür, *Leibniz Universität Hannover, Germany*

12:25 PM Closing Remarks



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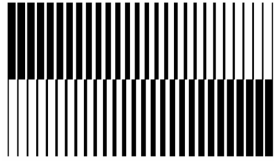
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