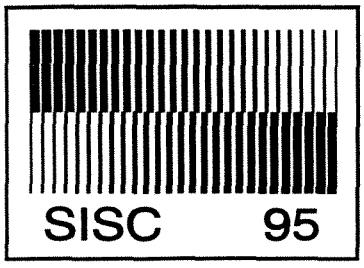

26th IEEE Semiconductor Interface Specialists Conference

7-9 December 1995
The Mills House, Charleston, South Carolina, USA

ABSTRACTS

General Chair: W. L. Warren

Technical Chair: R. E. Stahlbush

Arrangements Chair: D. A. Buchanan

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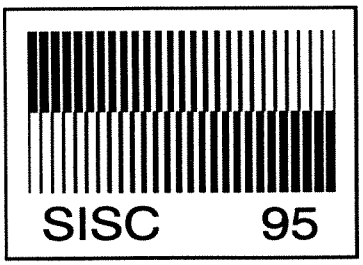

26th IEEE SISC

7-9 December 1995, Charleston, South Carolina, USA

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IN MEMORY OF EDWARD H. NICOLLIAN

The IEEE Semiconductor Interface Specialist Conference mourns the passing of Edward Haig Nicollian who died on December 17, 1994, in Charlotte, North Carolina at age 67. The SISC established a Student Best Paper Award in Ed's name to celebrate his numerous fundamental contributions to MOS device physics and technology, and to the SISC. Ed is survived by his wife and two sons.

Ed Nicollian received his M.A. in Physics from Columbia University, and then joined Bell Laboratories in 1957 where he was a member of the technical staff for 26 years. In 1983, he became Distinguished Professor of Electrical Engineering at the University of North Carolina at Charlotte (UNCC). He was a Fellow of IEEE and ECS.

Ed Nicollian's research contributions are known to most engineers and scientists interested in MOS device physics, technology, and characterization. He has made contributions in the areas of noise in MOS devices, avalanche injection in MOS capacitors, the conductance technique for measuring interface trap densities, MOS device characterization using the quasi-static technique, *C(V)* dopant profiling, the *Q-C* method, instabilities in MOS devices, MOSFET scaling, silicon oxidation kinetics, carrier confinement in quantum structures, and barrier-height characterization.

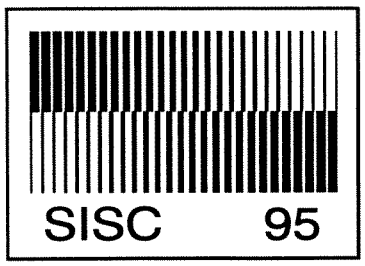
Ed Nicollian's contributions to education came even before he joined UNCC. In 1982, he wrote with J. Brews the tour-de-force monograph *MOS Physics and Technology*, published by J. Wiley and Sons, New York, NY. At UNCC, he founded his department's research and doctoral program in Electrical Engineering and Engineering Science, and principally contributed to the creation of the Cameron Center for Applied Research. He supervised numerous doctoral dissertations at UNCC, collaborated with researchers and colleagues at MCNC (Microelectronics Center of North Carolina), and taught an advanced graduate class on MOS device physics and characterization over the North Carolina Video Network which was attended by students at UNCC, UNC Chapel Hill, Duke University, and North Carolina State University.

At the Semiconductor Interface Specialists Conference, Ed Nicollian presented numerous talks, contributed to the technical program planning committee, and to the executive committee. He also served as the Technical Program Chairman of SISC in 1982.

I have had the pleasure and joy of knowing Ed Nicollian after I joined the Department of Electrical Engineering at Duke and the North Carolina microelectronics community at large, in 1983. We both spent summer of 1987 at MCNC, and over daily lunch breaks and several suppers, I witnessed Ed's sheer enthusiasm and genuine interest in the nature of all things. Whether the subject of discussion was interface traps at the $Si\text{-}SiO_2$ interface, silicon oxidation kinetics in the ultrathin regime, the mentor relationship of a professor with his graduate students, the relationship of fathers with their children, trout flyfishing on a remote stream in Pennsylvania, the events that shaped the course of history during the American Civil War, or the challenges of planting roses in his home soil at Charlotte, Ed Nicollian's whole-hearted enthusiasm and his instincts of the researcher were always present. He considered all angles, pursued all leads, and always reached strong opinions.

Edward Nicollian left our community with a legacy of excellence that will always be associated with the SISC Ed Nicollian Best Student Paper Award. I share the feeling of great loss with Ed's colleagues, friends, students, family members, and all those who had the luck of knowing him. His memory will always energize our pursuit of knowledge and excellence.

Hisham Z. Massoud
1994 SISC General Chairman
Department of Elec. and Comp. Engineering
Duke University, Durham, NC 27708-0291



26th IEEE SISC

7-9 December 1995, Charleston, South Carolina, USA

SESSION 1
Thin Oxides I
Thursday 12/7/95, 8:15 - 10:00 am

8:15 am Opening Remarks

8:30 am 1.1 **Structural and Electrical Characterization of Ultrathin Gate Oxides and Their Interfaces**, Masataka Hirose, Hiroshima University, Higashi-Hiroshima, Japan (Invited)

9:05 am 1.2 **Medium Energy Ion Scattering of Silicon Oxidation in the 5 - 80 Å Regime**, E. Garfunkel, E. P. Gusev, H. C. Lu, and T. Gustafsson, Rutgers University, Piscataway, NJ, USA (Invited)

9:40 am 1.3 **Direct Imaging of Ballistic-Emission Electrons from MOS Structures**, Marián Mankos, E. Cartier, M.C. Reuter, D.J. DiMaria, and R.M. Tromp, IBM T.J. Watson Research Center, Yorktown Heights, NY, USA

POSTERS P1.1 - P1.6, Oral Summary
Thursday, 12/7/95, 10:00 - 10:18 am

10:00 am P1.1 **The Use of Fowler-Nordheim Tunneling Current Oscillations To Obtain Ultra Thin SiO_2 Film Properties**, E.A. Irene, S. Zafar and K.J. Hebert, Department of Chemistry, University of North Carolina, Chapel Hill, NC, USA

10:03 am P1.2 **Thickness-Deconvolved Structural Properties of Thermally-Grown Silicon Film**, Kenji Ishikawa, Hiroki Ogawa, Sumiko Oshida, Kaina Suzuki, and Shuzo Fujimura, Processs Development Division, Fujitsu Limited, Kawasaki, Japan

10:06 am P1.3 **Microroughness of Clean Silicon Surfaces and Gate Oxide Breakdown**, M. Depas, B. Vermeire, P. W. Mertens, and M. M. Heyns, IMEC, Leuven, Belgium, A. Crossley and C. J. Sofield, AEA Technology, Oxon, UK

10:09 am P1.4 **The Effect of Stress Polarity on Cumulative Character of Oxide Wear-Out Under High-Field Injection**, Tomasz Brożek, Eric C. Szyper, and Chand R. Viswanathan, Elec. Engineering Dept., Univ. of California at Los Angeles, Los Angeles, CA, USA

10:12 am P1.5 **Interface States at Ultrathin Chemical Oxide/Si Interface for MOS Devices: XPS Measurements Under Biases**, Hikaru Kobayashi, Yoshiyuki Yamashita, Dept. of Chemistry, Faculty of Engineering Science, and Research Center for Photoenergetics of Organic Materials, Osaka University, Osaka, Japan, and Yasushiro Nishioka, Texas Instruments Tsukuba Research and Development Center Ltd., Japan

10:15 am P1.6 **Scaling Analysis of Hot Electron Related Phenomena for Two Competing Fully-Depleted SOI n-MOSFET's Using Monte Carlo Simulation**, R.B. Hulfachor, K.W. Kim, M.A. Littlejohn, and C.M. Osburn, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA

SESSION 2
SiC/Measurment Techniques
Thursday, 10:40 am - 12:15 pm

10:40 am 2.1 **Electrical Properties and Device Applications of Thermally Oxidized Silicon Carbide**, James A. Cooper, Jr., Purdue University, West Lafayette, IN, USA (Invited)

11:15 am 2.2 **Improved Oxidation Procedures for Reduced SiO_2/SiC Defects,** L. A. Lipkin and J. W. Palmour, Cree Research, Inc., Durham, NC, USA

11:35 am 2.3 **Energy Distribution of Electron States at SiC/SiO_2 Interfaces**, V.V. Afanas'ev, M. Bassler, G. Pensl, and M.J. Schulz, Institute of Applied Physics, University of Erlangen, Erlangen, Germany

11:55 am 2.4 **Equipment for Contactless and Sensitive Measuring the Electronic Properties of Semiconductor Surfaces and Interfaces and Results for Etched and H-Terminated Si-Surfaces and the Early Stages of Oxidation,** H. Flietner, Ngo Duong Sinh, H. Angermann, W. Fűssel, Hahn-Meitner-Institute, Dept. Photovoltaics, Berlin, Germany

POSTERS P2.1 - P2.5, Oral Summary
Thursday, 12/7/95, 12:15 - 12:30 pm

12:15 pm P2.1 **Studies of Two-Dimensional Roughness and Steps at Buried Si/SiO_2 Interface**, Xidong Chen and J. Murray-Gibson, Department of Physics, University of Illinois at Urbana-Champaign, Urbana, IL, USA

12:18 pm P2.2 **Silicon Surface Roughness as Measured by Atomic Force Microscopy and X-ray Scattering**, A. Munkholm, S. Brennan, Stanford Synchrotron Radiation Lab., Stanford Linear Accelerator Center, Stanford, CA, USA, and E.C. Carr, Hewlett-Packard Co., Palo Alto, CA, USA

12:21 pm P2.3 **The Influence of FN Stress on nMOSFETs Characterised Using Three Level Charge Pumping and 1/f Noise Measurements**, M.J. Kivi, X.J. Yuan, S. Taylor, Department of Electrical Engineering, University of Liverpool, Liverpool, UK, P. Hurley and S. Moran, NMRC, University College Cork, Cork, Ireland

12:24 pm P2.4 **Analysis of Interface-State-Induced Threshold Voltage Variation in LDD n-MOSFET's Using a New Oxide Damage Profiling Technique** G.-H. Lee and Steve S. Chung, Dept. of Electronic Engineering, National Chiao Tung University, Hsinchu, Taiwan, ROC

12:27 pm P2.5 **Properties of Interface Traps in JVD™ Silicon Nitride MNS Capacitors**, A. Mallik, X.W. Wang, T.P. Ma, Dept. of Electrical Engineering, Yale University, New Haven, CT, G.J. Cui, T. Tamagawa, B.L. Halpern, and J.J. Schmitt, Jet Process Corp., New Haven, CT, USA

SESSION 3
P_b Centers and Other Interface Traps
Thursday, 12/7/95, 2:00 - 3:20 pm

2:00 pm 3.1 **Revision of the Passivation of P_b Interface Defects in Standard Thermal (111) Si/SiO_2 with Molecular Hydrogen,** A. Stesmans, Dept. of Physics, Univ. Leuven, Leuven, Belgium

2:20 pm 3.2 **Passivation of P_b-centers at the $Si(111)/SiO_2$ Interface During Electrical Stress,** E. Cartier and J.H. Stathis, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, USA

2:40 pm 3.3 **Paramagnetic Interface Traps in High-Temperature Annealed $Si/SiO_2/Si$ Structures** K. Vanheusden, W.L. Warren, J.R. Schwank, D.M. Fleetwood, M.R. Shaneyfelt, P.S. Winokur, Sandia National Laboratories, Albuquerque, NM, USA, R.A.B. Devine, CNET-France Telecom, France

3:00 pm 3.4 **Characterization of Individual Interface Traps with Charge Pumping**, N.S. Saks, Naval Research Laboratory, Washington, D.C., USA, G. Groeseneken, and I. DeWolf, IMEC, Belgium

POSTERS P3.1 - P3. 5, Oral Summary
Thursday, 3:20 - 3:35 pm

3:20 pm P3.1 **Theory of Impurity Interactions in Silicon Dioxide**, W. Beall Fowler, Kenneth C. Snyder, Dept. of Physics and Sherman Fairchild Lab., Lehigh Univ., Bethlehem, PA, USA, and Arthur H. Edwards, Dept. of Electrical Eng., Univ. of North Carolina at Charlotte, NC, USA

3:23 pm P3.2 **Analysis of Tunneling Through MOS Structures via Bohm Trajectories,** X. Oriols, F. Martín, and J. Suñé, Dept. de Física, Universitat Autònoma de Barcelona, Spain

3:26 pm P3.3 **Characterisation of a LPCVD Si_3N_4 Surface for Improved ISFET Performance**, A. Garde, J. Alderman, and W. Lane, National Microelectronics Research Centre, University College Cork, Ireland

3:29 pm P3.4 **Annihilation of Interface Traps by Hot-Electron Injection**, Yujun Li and T.P. Ma, Center for Microelectronic Materials & Structures and Dept. of Electrical Engineering, Yale University, New Haven, CT, USA

3:32 pm P3.5 **Oxide-nitride-oxide/Si (111) Interfaces Analyzed by Optical Second Harmonic Generation**, Kohji Watanabe, Microelectronics Research Lab., NEC Corp., Masato Kawata, Eiji Hasegawa, ULSI Device Development Lab., NEC Corp., and Hiroyuki Hirayama, Dept. of Materials Science and Engineering, Tokyo Institute of Technology, Japan

SESSION 4
Interface and Oxide Defects
Thursday, 12/7/95, 4:00 - 5:20 pm

4:00 pm 4.1 **Hole Trapping due to Local Distortion and Impurities in Amorphous Silicon Dioxide** Chioko Kaneta, Fujitsu Laboratories Ltd., Atsugi, Japan

4:20 pm 4.2 **On the Temperature Dependence of the Charge Build-up Mechanisms in Thin Oxides** E. Vincent, C. Papadas, SGS-THOMSON Microelectronics, Crolles, and G. Ghibaudo, Laboratoire de Physique des Composants à Semiconducteurs ENSERG, Grenoble, France

4:40 pm 4.3 **Hole Trap Analysis in Si/SiO_2 Structures by Electron Tunnelling,** M. Schmidt, S. Scharf, D. Braunig, Hahn-Meitner-Institut Berlin, Department of Applied Physics, Berlin, Germany

5:00 pm 4.4 **Interface State Generation Post Substrate Hot Hole Injection**, I.S. Al-kofahi and J.F. Zhang, Department of Electrical and Electronic Engineering, Liverpool John Moores University, Liverpool, UK, and G. Groeseneken, IMEC, Belgium

POSTERS P4.1 - P4.5, Oral Summary
Thursday, 5:20 - 5:35 pm

5:20 pm P4.1 **Generation of Electron Traps by VUV Radiation in Buried Oxides of SOI Structures**, V.V. Afanas'ev, University of Saint-Petersburg, Russia, A.G. Revesz, Revesz Associates, MD, USA, and H.L. Hughes, Naval Research Laboratory, Washington, DC, USA

5:23 pm P4.2 **Dynamics of Point Defect Relaxations Induced by Charge Trapping Reactions in Amorphous SiO_2**, V.A. Mashkov and R.G. Leisure, Department of Physics, Colorado State University, Fort Collins, CO, USA

5:26 pm P4.3 **Post-Irradiation Behavior of N_2O Annealed SiO_2/Si Interface**, Brian M. Dugan and T.P. Ma, Dept. of Electrical Engineering, Yale University, New Haven, CT, USA

5:29 pm P4.4 **Simulation for the Degradation of Flash Memory due to Charge Trap in the Tunnel Oxide**, A. Yokozawa, H. Shirai, K. Tsunenari, NEC ULSI Device Development Lab., Kanagawa, and T. Okazawa, NEC LSI Memory Division, Kanagawa, Japan

5:32 pm P4.5 **Influence of the Polysilicon / Oxide Interface on the CV Characteristics of n+ Polysilicon / Oxide / Silicon Capacitor Structures**, P.K. Hurley, S. Moran, and A. Mathewson, NMRC, University College Cork, Lee Maltings, Cork, Ireland, A. Kalnitsky, and A. Lepert, Centre Commun, CNET, France

SESSION 5
Thin Oxides II
Friday, 12/8/95, 8:15 - 9:50 am

8:15 am 5.1 **Transport Issues of STM-Injected Hot Electrons in Metal-Oxide-Semiconductor Structures**, R. Ludeke, E. Cartier, and A. Bauer, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA (Invited)

8:50 am 5.2 **Breakdown and Instability of 3 nm Gate Oxide**, M. Depas, B. Vermeire, and M. M. Heyns, IMEC, Leuven, Belgium

9:10 am 5.3 **Weak Fluence Dependence of Charge Generation in Ultra-thin Oxides on Silicon** K.R. Farmer, C.P. Debauche, A.R. Giordano, Dept. of Physics, New Jersey Institute of Technology, Newark, NJ, USA, P. Lundgren, M.O. Andersson, Dept. of Solid State Electronics, Chalmers University, Gothenburg, Sweden, and D.A. Buchanan, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, USA

9:30 am 5.4 **Separation of Impact Ionization and Anode Hole-Injection in the Si/SiO_2 Structure Using Monte Carlo Simulations** D.J. DiMaria and E. Cartier IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, USA

SESSION 6
Slow States, APC, Border Traps ...
Friday, 10:20 am - 12:15 pm

10:20 am 6.1 **Molecular Engineering using Thin Organic Films**, M. C. Petty, University of Durham, Durham, United Kingdom (Invited)

10:55 am 6.2 **Fast and Slow Border Traps in MOS Devices**, D.M. Fleetwood, W.L. Warren, J.R. Schwank, P.S. Winokur, M.R. Shaneyfelt, and L.C. Riewe, Sandia National Laboratories, Albuquerque, NM, USA

11:15 am 6.3 **Electron Spin Resonance Evidence for the Structure of a Switching Oxide Trap**, John F. Conley and Patrick M. Lenahan, The Pennsylvania State University, Dept. of Engineering Science and Mechanics, University Park, PA, USA Aivars J. Lelis and Timothy R. Oldham, Army Research Laboratory, Adelphi, MD, USA

11:35 am 6.4 **A Theoretical Study of the E′ Center as a Switching Trap**, Arthur H. Edwards, Dept. of Electrical Engineering, University of North Carolina at Charlotte, Charlotte, NC, USA and W.B. Fowler, Dept. of Physics and the Sherman Fairchild Laboratory, Lehigh University, Bethlehem, PA, USA

11:55 am 6.5 **Anomalous Positive Charge and E′ Centers in Atomic Hydrogen Exposed SiO_2**, J.H. Stathis and E. Cartier, IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, USA

SESSION 7
Dielectrics Other Than Thermal Oxide
Saturday, 12/9/95, 8:15 - 9:50 am

8:15 am 7.1 **Science and Technology in the Development of Thin Film Transistor Liquid Crystal Displays**, J. Batey, Xerox PARC, Palo Alto, CA (Invited)

8:50 am 7.2 **Current Transport in Ultrathin JVD™ Silicon Nitride Films**, Y. Shi, X.W. Wang, and T.P. Ma, Dept. of Electrical Engineering, Yale University, New Haven, CT, USA, G.J. Cui, T. Tamagawa, B.L. Halpern, and J.J. Schmitt, Jet Process Corporation, New Haven, CT, USA

9:10 am 7.3 **Experimental Evidence for the Relationship Between an SiO_2 Defect and Oxygen Deficiency During High Temperature Annealing** T.L. Chen, M.E. Zvanut, University of Alabama at Birmingham, USA, R.E. Stahlbush and E.S. Steigerwalt, Naval Research Laboratory, Washington, DC, USA

9:30 am 7.4 **MOSFET Gate Oxide Degradation by Localized Pure Hot-Hole Injection**, Shankar P. Sinha, A. Zaleski, Dimitris E. Ioannou, ECE Dept., George Mason University, Fairfax, VA, USA, William C. Jenkins, George J. Campisi, and Harold L. Hughes, Naval Research Laboratory, Washington, D.C., USA

SESSION 8
Nitrogen Containing Oxides
Saturday, 10:20 am - 12:15 pm

10:20 am 8.1 **Atomic Structure and Electrical Properties of Nitrided Si-SiO_2 Interfaces**, G. Lucovski, D. R. Lee, Z. Jing, C. Parker and J. R. Hauser, North Carolina State University, Releigh, NC, USA (Invited)

10:55 am 8.2 **Kinetics of Nitrogen Incorporation and Removal in N_2O-Oxides Grown by Rapid Thermal Oxidation**, M.L. Green, T.W. Sorsch, L.C. Feldman, AT&T Bell Laboratories, Murray Hill, NJ, USA, and H.S. Luftman, AT&T Solid State Technology Center, Breinigsville, PA, USA

11:15 am 8.3 **Gas Phase Chemistry of N_2O Furnace Oxidation**, K.A. Ellis and R.A. Buhrman, School of Applied and Engineering Physics, Cornell University, Ithaca, NY, USA

11:35 am 8.4 **A Self Consistent Physical Explanation for the Mobility Behavior of n-Channel and p-Channel MOSFET's with Oxynitride Gate Dielectrics Formed by Low-Pressure Rapid Thermal Chemical Vapor Deposition**, E.M. Vogel, W.L. Hill, V. Misra, P.K. McLarty, J.J. Wortman, J.R. Hauser, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, USA, P. Morfouli, G. Ghibaudo, and T. Ouisse, Laboratoire de Physique des Composants à Semiconducteurs -ENSERG, Grenoble, France

11:55 am 8.5 **Barrier Height Measurements on O_2 and N_2O Gate Dielectrics**, B.E. Weir, K.S. Krisch, D. Monroe, K.W. Evans-Lutterodt, M.L. Green, D. Brasen, AT&T Bell Laboratories, Murray Hill, NJ, USA, H. Nussbaumer, University of Konstanz, Konstanz, Germany, M.-T. Tang, SRRC, Hsinchu, Taiwan, ROC, L. Manchanda, AT&T Bell Laboratories, Holmdel, NJ, USA